DR. AMBEDKAR INSTITUTE OF TECHNOLOGY, BANGALORE

(An Autonomous Institution Affiliated to VTU, Belgaum)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LIST OF MEMBERS FOR BOARD OF STUDIES for the Academic year 2019-21

Date:11-05-2019

Sl No.	*CATEGORY*	*Nomination of the Committee*	*Name of the Person with Designation*	*Signature*
1	Head of the Department	Chairperson	Dr. Jayaramaiah.G.V. Professor and Head Department of ECE, Dr.AIT Bengaluru-56	Jayaramaiah G
2	Faculty Members at Different Levels Bearing Different Specializations	Member 1.	Dr.Umadevi.H Professor, Dept. of ECE, Dr. AIT, Bengaluru-56	~~ABS~~ OOD
		Member 2.	Dr. Mahalinga V Mandi. Professor Dept of ECE, Dr.AIT, Bengaluru-56	OOD
		Member 3.	Smt. Akalpita L Kulkarni Dept of ECE, Dr. AIT, Bengaluru-56 Assoc. Professor Dept of ECE, Dr AIT, Bengaluru-56	Akulkarni 11/5/19
		Member 4.	Dr. Ramesh.S Professor, Dept of ECE, Dr.AIT, Bengaluru-56, Bengaluru-56	11.5.19
		Member 5.	Smt. Sudha.B.S. Associate Professor Dept of ECE, Dr.AIT. Bengaluru-56	Sudha.B.S 11/5/19
		Member 6.	Dr.Shivaputra Assistant Professor Dept of ECE, Dr.AIT, Bengaluru-56	
		Member 7.	Dr. Jambunath S Baligar Associate Professor Dept of ECE, Dr.AIT, Bengaluru-56	
		Member 8.	Dr.Chetan.S Assistant Professor, Dept of ECE, Dr.AIT, Bengaluru-56	
3	Subject Experts from outside the College	Member 1.	Dr. Devendra Jalihal Professor, EEE department IIT Madras, Chennai-600 036	

8	Post Graduate Meritorious alumnus nominated by Principal	Member	Mr. Kubendra.K Senior Design Engineer VLSI Group Samsung ,India,Outer ring Road, Near Marathahalli Bengaluru	
9	Student Representatives	Member	Keerthana N 1DA18EC064 1st Year ECE. UG Student	
10		Member	Vishaka bhat 1DA17ec155 2nd Year, ECE UG Student	
11		Member	Vidhee L 1DA17EC150 2nd Year, ECE UG Student	Vidhee L
12		Member	Sharath N 1DA16EC108 3rd Year, ECE UG Student	Sharath N.
13		Member	Bharath K 1DA16EC144 3rd Year, ECE UG Student	
14		Member	Heera P 1DA16EC041 3rd Year, ECE UG Student	
15		Member	Kumudini G 1DA15EC072 4th Year, ECE UG Student	
16		Member	Pranav Jayaram 1DA15EC105 4th Year, ECE UG Student	
17		Member	Arpitha B V 1DA17LVS02 2nd Year, M.Tech. PG Student	Arpitha.BV
18		Member	Chinthana K S 1DA17LVS04 2nd Year, M.Tech. PG Student	

Dr.Ambedkar Institute of Technology, Bengaluru-56

(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi)

Department of Electronics and Communication Engineering

M.Tech. in VLSI Design and Embedded Systems

BOS Meeting

BOS meeting for the academic year 2019-20 conducted at SJB Seminar Hall-001, Dr. AIT campus on Saturday 11th May 2019, 11 AM and the following are the points discussed:

Minutes of the Meeting

1. System Verilog should be core subject (19LVS151).
2. Digital system design using Verilog should be core subject (19LVS152).
3. Subject -18LVS154 to be made a core subject.
4. Add VLSI methodology with respect to analog, digital, SoC design and SoC verification.
5. Mathematics subject should not be necessarily a compulsory.
6. In advanced embedded system – add EDK tools, add advanced topics on hardware and software design.
7. SEE should be introduced for minor project / technical seminar.
8. Mathematics subject should have VLSI subject related topics.
9. Include one elective related to subject machine intelligence/machine learning/artificial intelligence.
10. Add recent topics in all the fields.
11. As far as possible try to use open source for practical.
12. Avoid the text books prior to 2014 edition.
13. In mathematics probability and random variables topic is not suitable for VLSI subjects (linear algebra and differential equations).
14. Include Nano-Electronics subject.
15. Change the subject name of CMOS VLSI design to Microelectronics.

PG Coordinator

HOD

Dept. of Electronics and Communication Engg.,
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

Minutes of Board of Studies (BOS) Meeting:

The Meeting of Board of Studies (BOS) for PG, Department of Electronics and Communication Engineering was held on 20-08-2020 at 10:30 a.m. under the Chairmanship of the Dr. Ramesh S, Professor and Head, Department of Electronics and Communication Engineering on Digital Platform Google Meet with meeting-link: https://meet.google.com/ozd-eisw-bqy.

At the very outset, the Chairman welcomed all the Internal and External members of BOS to the meeting and gave a preliminary presentation on the agenda items with reference to the scheme and syllabus of PG for the academic year 2020-21
The chairman along with academic coordinator(s) gave a detailed presentation of the courses to be offered to the students in both Core and Elective subjects in semester wise at the Post Graduate level and also briefed the members about the Curriculum Design of the Department for the PG Course.

PROCEEDINGS/RESOLUTIONS:

The following are the Suggestions of the members of BOS with reference to the presentations:

1. Subjects related to Artificial Intelligence and Machine learning to be incorporated suggested by Dr. Santanu Mahapatra from IISC.

   Sol. Incorporated as an elective subject for the third semester

2. Suggested by many BOS members, students should carry out the project work for full one year for that internship need to be completed before the commencement of the 3rd semester.

   Sol. Internship will be scheduled during the third semester and vacation to provide the maximum time to carry out the project work also

BOS P G Coordinators	Signatures
1. Dr. J S Baligar	
2. Dr. Chetan S	

Professor & Head
BOS Chairman

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

Minutes of Board of Studies (BOS) Meeting:

The Meeting of Board of Studies (BOS) of department Electronics and Communication Engineering was held on 19-06-2021 at 11:00 a.m. under the Chairmanship of the Dr.Ramesh S,Professor andHead, Department of Electronics and Communication Engineeringon Digital Platform Google Meet with meeting-id: **meet.google.com/oek-ffdx-ngs**

At the very outset, the Chairman welcomed all the Internal and External members of BOS to the meeting and gave a preliminary presentation on the agenda items with reference to the scheme and syllabus of PG for the academic year 2022-23.

The chairman along with academic coordinator(s) gave a detailed presentation of the courses to be offered to the students in both Core and Elective subjects in semester wise at the PostGraduate level and also briefed the members about the Curriculum Designof the Department for the PG Course.

PROCEEDINGS/RESOLUTIONS:

The members of BOS suggested to make no changes to the submitted syllabus and approved the syllabus as it is.

CHAIRMAN
BOS Dept. of ECE

BOS Coordinators	**Signatures**
1. **Dr. J S Baligar**	
2. **Dr. Chetan S**	

Subject Title: **ANALOG IC DESIGN**		
Subject Code**: LVS21**	No. of Credits**: 3=4:0:0(LTP)**	No. of lecture hours/week **:04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar) + SEE **= 40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1 Understand the MOSFET operations in detail.
2 Understand the small signal circuit concepts of MOSFET.
3 Analysis of analog circuits parameters based on the small signal circuits.
4 Applications OP-Amp in an analog building blocks.
5 Design and develop ADC and DAC using different architectures.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Basic MOS Device Physics:** General considerations, MOS I/V Characteristics, second order effects, MOS device models. **Single stage Amplifier:** CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models. **[Text 1]**	10	L1,L2, L3,
2	**Differential Amplifiers:** Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. **Passive and active Current mirrors:** Basic current mirrors, Cascade mirrors, active current mirrors. **[Text 1]**	10	L1,L2, L3, L4
3	**Frequency response of CS stage:** source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair. **[Text 2]**	10	L1,L2, L3, L4
4	**Operational Amplifiers:** One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of 2stage OP-Amp, Other compensation techniques. **Oscillators:** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. **PLL:** Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. **Band gap References** and Switched capacitor filters. **[Text 2]**	12	L1,L2, L3, L4
5	**Data Converter Architectures:** DAC & ADC Specifications, (Qualitative Analysis of)Resistor String DAC, R-2R Ladder Networks, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. **[Text 3]**	10	L1,L2, L3, L4

Note: Each Unit will have internal choice.

COURSE OUTCOMES:

CO1 Model the MOSFET using small signal and large signal analysis

CO2	Design the CMOS VLSI circuits.
CO3	Analysis of the CMOS analog circuits.
CO4	Synthesis of the NMOS analog circuits using PSPICE Models
CO5	Design analog to digital and digital to analog circuits using NMOS and PMOS transistors
CO6	Design OPAMP circuit

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3
CO3	PO4,PO5
CO4	PO5,PO6
CO5	PO6,PO7
CO6	PO1,PO2,PO3,PO7

TEXT BOOK

1. BehzadRazavi, Design of Analog CMOS Integrated Circuits", , TMH, 2007.
2. R.JacobBaker, CMOS Circuit Design, Layout, and Simulation, Second Edition, Publisher: Wiley-IEEE Press, 1997.
3. Phillip E. Allen, Douglas R. Holberg, CMOS Analog Circuit Design, Second Edition, Oxford University Press, 2002.

REFERENCE BOOKS/WEBLINKS

1. Philip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2nd Edition, 2004.
2. nptel.ac.in/courses/117106093/.

Subject Title: **ASIC Design**		
Subject Code: **18LVS251**	No. of Credits**:3=4:0:0(L:T:P)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1. Explain ASIC methodologies and programmable logic cells to implement a function on IC.
2. Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
3. Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
4. Design CAD algorithms and explain how these concepts interact in ASIC design

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Introduction To ASICs**, Full Custom, Semi-Custom and Programmable ASICS, ASIC Design Flow, ASIC Cell Libraries. **CMOS Logic:**Datapath Logic Cells: Datapath Elements, Adders: Carry Skip, Carry Bypass, Carry Save, Carry Select, Conditional Sum, Multiplier (Booth Encoding), Data Path Operators, I/O Cells.**[TEXT1]**	10	L1,L2, L3
2	**ASIC Library Design:** Logical Effort: Predicting Delay, Logical Area and Logical Efficiency, Logical Paths, Multi Stage Cells, Optimum Delay and Number Of Stages. **Programmable ASIC Logic Cells:** MUX as Boolean Function Generators, Actel ACT: ACT 1, ACT 2 And ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.**[TEXT1]**	10	L1,L2, L3
3	**Programmable ASIC I/O Cells:** Xilinx and Altera I/O Block. **Low-Level Design Entry:** Schematic Entry: Hierarchical Design, Netlist Screener. **ASIC Construction:** Physical Design, CAD Tools. **Partitioning:** Goals and Objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead Algorithms. **[TEXT1]**	10	L1,L2, L3, L4
4	**Floor Planning and Placement:** Goals and Objectives, Floor Planning Tools, Channel Definition, I/O And Power Planning and Clock Planning. **Placement:** Goals and Objectives, Min-Cut Placement Algorithm, Iterative Placement Improvement, Physical Design Flow. **[TEXT1]**	10	L1,L2, L3, L4
5	**Routing:** Global Routing: Goals and Objectives, Global Routing Methods, Back-Annotation. Detailed Routing: Goals and Objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit Extraction and DRC. **[TEXT1]**	12	L1,L2, L3, L4

Note: Each Unit will have internal choice.

COURSE OUTCOMES:

CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
CO2	Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.
CO4	Understand and identify different Programmable ASIC Logic Cells.
CO5	Create floor plan including partition and routing with the use of CAD algorithms.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2, PO3,PO4,PO5
CO3	PO2,PO3,PO4,PO5
CO4	PO2,PO3, PO4,PO5
CO5	PO3,PO4, PO5,PO6

TEXT BOOK

1. Michael John Sebastian Smith, “Application - Specific Integrated Circuits” Addison Wesley Professional; 2005.

REFERENCE BOOKS/WEBLINKS

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd edition, Addison Wesley/ Pearson education, 2011.
2. VikramArkalgudChandrasetty,”VLSI Design: A Practical Guide for FPGA and ASIC Implementations”, Springer, 2011, ISBN: 978-1-4614-1119-2.
3. RakeshChadha, Bhasker J., “An ASIC Low Power Primer”, Springer, ISBN: 978-1-4614-4270-7.

Subject Title: **DIGITAL IC DESIGN**		
Subject Code: **LVS14**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives: This course will enable the students to:

1. Learn circuit-oriented approach towards digital design
2. Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
3. Infer different approaches to digital timing and clocking circuits
4. Understand the impact of clock skew on the behaviour of digital synchronous circuits
5. Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Implementation Strategies For Digital ICS**: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	12	L1,L2, L3,
2	**Coping With Interconnect**: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	10	L1,L2, L3
3	**Timing Issues In Digital Circuits**: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Based Clocking, SelfTimed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	10	L1,L2, L3, L4

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
4	**Designing Memory and Array Structures**: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Non-volatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control.	10	L1,L2, L3, L4
5	**Designing Memory and Array Structures:** Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.	10	L1,L2, L3, L4

Note: Each Unit will have internal choice.

COURSE OUTCOMES: After studying this course, students will be able to:

CO1 Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.

CO2 Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability

CO3 Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.

CO4 Infer the reliability of the memory

CO5 Solve application specific integrated circuit problems

CO6 Design effective arithmetic building blocks

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7,PO8
CO5	PO3,PO4
CO6	PO3,PO4,PO5

TEXT BOOK

1. Jan M Rabey, Anantha Chandrakasan, BorivojeNikolic, ―Digital Integrated Circuits-A Design Perspective‖, PHI, 2nd Edition

REFERENCE BOOKS/WEBLINKS

1. M. Smith, ―Application Specific Integrated circuits‖, Addison Wesley, 1997
2. H. Veendrick, ―MOS IC‘s: From Basics to ASICs, Wiley-VCH, 1992.
3. Anantha P. Chandrakasan , Robert W. Brodersen, ―Low Power Digital CMOS Design‖, Kluwer Academic Publisher, 1995.

Subject Title: **EMBEDDED OS**		
Subject Code: **LVS24**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1 Introduce the fundamental concepts of Embedded Operating Systems and the real time embedded system.

2 Apply concepts relating to operating systems such as Scheduling techniques, Dynamic priority policies.

3 Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.

4 Study programs for multithreaded applications using suitable techniques.

5 Discuss embedded system components, Debugging components and file system components.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Real-Time Systems and Resources:**Brief history of Real Time Systems, A brief history of Embedded Systems. Resource Analysis, Real-Time Service Utility, scheduling classes, Scheduler concepts, Real-Time OS, State transition diagram. (Text 1)	10	L1,L2, L3,
2	**Processing with Real Time Scheduling:** Introduction, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams, Problems and issues, Feasibility, Rate Monotonic least upper bound (No derivation), Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies. (Text 1)	10	L1,L2, L3
3	**I/O Resources**: Worst case execution time, Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, Shared Memory, ECC Memory, **Multi-resource Services:** Blocking, Deadlock and livelock, Priority inversion. **Soft real-time services:** Missed deadline, QoS. (Text 1)	11	L1,L2, L3
4	**Embedded OS Concepts:** Semaphores, Mutex, Mailboxes, Message queues, Pipes, Process and thread creations, Simple Programs, Multithreading, Programs related to semaphores, message queue, Examples of Embedded OS. (Text 2)	10	L1,L2, L3, L4
5	**Firmware Components:** The 3 firmware components, Single step debugging, Test access ports, Trace Ports.	11	L1,L2, L3, L4

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
	Performance Tuning: Basic concepts of Drill-Down tuning, Fundamental Optimizations. **High Availability and Reliability Design:** Reliability and Availability, Similarities and Differences, Reliability, Reliable software, available software, Design Trade-offs. (Text 1)		

Note: Each Unit will have internal choice.

COURSE OUTCOMES:

CO1 Discuss the various real time services, real time service utilities, Apply priority based static and dynamic real time scheduling techniques for the given specifications.

CO2 Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory) to improve the system performance.

CO3 Analyze deadlock conditions, shared memory problem, priority inversion, missed deadlines and QoS.

CO4 Develop the programs for multithreaded applications using suitable techniques.

CO5 Summarize the concepts of Firmware components, performance tuning, High Availability and Reliability Design.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO1,PO2,PO4,PO5
CO3	PO1,PO2,PO3,PO5,PO6,PO8
CO4	PO1,PO2,PO5,PO6,PO7,PO9
CO5	PO1,PO2,PO5,PO6,PO7, PO8, PO9

TEXT BOOK

1. "**Real-Time Embedded Systems and Components",** Sam Siewert, Cengage Learning India Edition, 2007.
2. "**Embedded/Real-time Systems**", Dr K.V.K.K. Prasad, Dreamtech press, 2017.

REFERENCE BOOKS/WEBLINKS

1. James W S Liu, "**Real Time System**", Pearson education, 2008.
2. nptel.ac.in/courses.

Subject Title: **Embedded System Design with FPGA**		
Subject Code: **18LVS322**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **:04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **30+(10+10)+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1 Explain the computer hardware and software.

2 Describe the concept of Field Programmable gate arrays.

3 Explain the Embedded system design tools and design prototyping.

4 Describe the various concept of design of utility hardware cores.

5 Explain the concepts of Embedded design steps.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Computer Hardware And Software:** Computer System, Computer Software, Machine Language, Assembly Language, High-Level Language, C Programming Language, Instruction Set Architecture, SMPL-CPU Design, CPU Specification, Single-Cycle Implementation, Multi-Cycle Implementation, SAYEH Design and Test, Details of Processor Functionality, SAYEH Datapath, SAYEH Verilog Description, SAYEH Top-Level Testbench / Assembler, SAYEH Hardware Realization.	10	L1,L2, L3,
2	**Field Programmable Devices:** Read Only Memory, Basic ROM Structure, NOR Implementation, Distributed Gates, Array Programmability, Memory View, ROM Variations, Programmable Logic Arrays, PAL Logic Structure, Product Term Expansion, Three-State Outputs, Registered Outputs, Commercial Parts, Complex Programmable Logic Devices, Altera's MAX 7000S CPLD, Field Programmable gate arrays, Altera's FLEX 10K FPGA, Altera's cyclone FPGA.	10	L1,L2, L3,
3	**Tools For Design And Prototyping:** Hardware Design Flow, Datapath of Serial Adder, Serial Adder Controller, HDL Simulation and Synthesis, Pre-Synthesis Simulation, Module Synthesis, Post-Synthesis Simulation, Mixed-Level Design with Quartus II, Project Specification, Block Diagram Design File, Creating and Inserting Design Components, Wiring Design Component, Design Compilation, Design Simulation, Synthesis Results, Design Prototyping, UP3 Board Specification, DE2 Board Specification, Programming DE2 Cyclone II.	10	L1,L2, L3
4	**Design Of Utility Hardware Cores:** Library Management, Basic IO Device Handling, Debouncer, Single Stepper, Utilizing UPS Basic IO, Utilizing DE2 Basic IO, Frequency Dividers, Seven Segment Displays, SSD Driver, Testing DE2 SSD Driver, LCD Display Adapter, Writing into LCD, LCD Initialization, Display Driver with Initialization, Testing the LCD Driver (UPS), Testing the LCD Driver (DE2), Keyboard Interface Logic, Serial Data Communication, Power-On Routine, Codes and Commands, Keyboard Interface Design, VGA Interface Logic, VGA Driver Operation, Monitor Synchronization Hardware, Character Display, VGA Driver for Text Data, VGA Driver Prototyping (UPS), VGA Driver Prototyping (DE2). **Design With Embedded Processors:** Embedded Design Steps, Processor Selection, Processor Interfacing, Developing Software, Filter Design, Filter Concepts, FIR Filter Hardware Implementation, FIR Embedded Implementation,	11	L1,L2, L3, L4

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
	Building the FIR Filter, Design of a Microcontroller, System Platform, Microcontroller Architecture.		
5	**Design Of An Embedded System:** Designing an Embedded System, Nios II Processor, Configurability Features of Nios II, Processor Architecture, Instruction Set,Nios II Alternative Cores, Avalon Switch Fabric, Avalon Specification, Address Decoding Logic, Data-path Multiplexing, Wait-state Insertion, Pipelining, Endian Conversion, Native Address Alignment and Dynamic Bus Sizing, Arbitration for Multi-Master Systems, Burst Management, Clock Domain Crossing, Interrupt Controller, Reset Distribution, SOPC Builder Overview, Architecture of SOPC Builder Systems, Functions of SOPC Builder, IDE Integrated Development Environment, IDE Project Manager, Source Code Editor, C/C++ Compiler, Debugger , Flash Programmer, An Embedded System Design: Calculator, System Specification, Calculating Engine, Calculator IO interface, Design of Calculating Engine, Building Calculator Software, Calculator Program, Completing the Calculator System.	11	L1,L2, L3, L4

Note: Each Unit will have internal choice

COURSE OUTCOMES

CO1 Describe the concept of Machine Language, Assembly Language, High-LeveI Language.

CO2 Analyze the concept of SAYEH Top-Level Testbench / Assembler.

CO3 Describe the structure of PLA and PAL arrays.

CO4 Discuss the concept of Altera's MAX 7000S CPLD.

CO5 Evaluate the HDL Simulation and Synthesis.

Course outcome and program outcome mapping

CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO12

TEXT BOOKS:

1. Embedded Core Design with FPGAs**,** 1e, Zainalabedin Navabi, McGrawHill 2008.

REFERENCE BOOKS:

1. Embedded Systems Design with FPGAs, Athanas, Peter, Pnevmatikatos, Dionisios, Sklavos, Nicolas, Springer, 2013.

Subject Title: **NETWORK SECURITY AND CRYPTOGRAPHY**		
Subject Code: **18LVS252**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1 Identify and utilize different forms of cryptography techniques.

2 Incorporate authentication and security in the network applications.

3 Distinguish among different types of threats to the system and handle the same.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Security** – Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques **[TEXT1]**	12	L1,L2, L3,
2	**Number Theory** - Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic. **[TEXT1]**	10	L1,L2, L3, L4
3	**Private-Key (Symmetric) Cryptography** - Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis. **[TEXT1]**	10	L1,L2, L3, L4
4	**Public-Key (Asymmetric) Cryptography** - RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC. **[TEXT1]**	10	L1,L2, L3, L4
5	**Authentication** - IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction. **System Security** - Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.	10	L1,L2, L3, L4

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
	[TEXT1]		

Note: Each Unit will have internal choice.

COURSE OUTCOMES:

CO1	Define the basic concepts of network security, classical encryption, number theory, Private key, public key, authentication and network security
CO2	Understand the structures of cryptographic algorithms and their applications.
CO3	Apply the concept of classical encryption techniques to existing standard algorithms.
CO4	Illustrate the significance of cryptographic algorithms and their applications in network security.
CO5	Design the private key and public key, authentication functions for applications in network security.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO6
CO2	PO1,PO2,PO6, PO10
CO3	PO1,PO2
CO4	PO1,PO2,PO6,PO10
CO5	PO1,PO2, PO6,PO10

TEXT BOOK

1. William Stallings, “Cryptography and Network Security, Principles and Practices”, Pearson Education, 3rd Edition.

REFERENCE BOOKS/WEBLINKS

1. Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private Communication in a Public World”, Prentice Hall, 2nd Edition
2. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, “Security Architecture, Design Deployment and Operations”, RSA Pres,
3. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey,

"Inside Network Perimeter Security", Pearson Education, 2nd Edition

4. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident.Detection and Response", William Pollock Publisher, 2013.

Subject Title: **PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE**		
Subject Code: **LVS154**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

This course will enable the students to:

1. Write an embedded C application of moderate complexity.
2. Develop and analyse algorithms in C++.
3. Differentiate interpreted languages from compiled languages.
4. Understanding of various scripting languages.
5. Development of firmware for embedded system.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Embedded 'C' Programming** - Bitwise operations, Dynamic memory allocation, OS services - Linked stack and queue, Sparse matrices, Binary tree - Interrupt handling in C, Code optimization issues - Writing LCD drives, LED drivers, Drivers for serial port communication - Embedded Software Development Cycle and Methods (Waterfall, Agile)	10	L1,L2,L3.
2	**Object Oriented Programming** - Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism, CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer,	12	L1,L2,L3.
3	**Constructors, destructors, friend function, dynamic memory allocation, Overloading and Inheritance**: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions	10	L1,L2,L3.
4	**Templates:** Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.	10	L1,L2,L3

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
5	**Scripting Languages Overview of Scripting Languages** – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.	10	L1,L2,L3

Note: Each Unit will have internal choice.

COURSE OUTCOMES:

CO1	Able to develop embedded C application of moderate complexity.
CO2	Able to develop and analyse algorithms in C++
CO3	To choose between the compiled and interpreted language.
CO4	Can take decision to choose best scripting language
CO5	Able to write firmware for embedded systems.

Course outcome and program outcome mapping

CO1	PO3,PO4
CO2	PO3,PO4
CO3	PO3,PO4,
CO4	PO3,PO4
CO5	PO3,PO4

TEXT BOOK/ REFERENCE BOOKS/WEBLINKS

1. Michael J. Pont , “Embedded C”, Pearson Education, 2nd Edition, 2008
2. Michael Berman, “Data structures via C++”, Oxford University Press, 2002
3. Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition 2011
4. Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999

5 Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey & Sons, 2005.

Subject Title: **STATIC TIMING ANALYSIS**		
Subject Code: **18LVS323**	No. of Credits:**4=4:0:0(LTP)**	No. of lecture hours/week **:04**
Exam Duration: 03 **Hours**	CIE +(Assignment+Seminar) + SEE = **20+10+70=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1 Understand timing analyses at various process, environment and interconnect corners.

2 Apply the learnt concepts of STA to evaluate the delay of the circuits.

3 Understand and analyse the signal integrity issues for the IC. Generate the timing analysis report using EDA tool.

4 Understand verification and analyze the generated report to identify issues for the violation

5. Learn different techniques to meet timing in an IC design. Set up the timing analysis environment and perform the timing analysis for various cases.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Introduction**: Nanometer Designs, What is Static Timing Analysis?. Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations, **STA Concepts**: CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions .	10	L1,L2
2	**Standard Cell Library**: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, TimingModels - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setup and Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State-Dependent Models XOR, XNOR and Sequential Cells, Interface Timing Model for a Black Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage,, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and Sequential Cells, Other Noise	10	L1,L2

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
	Models, Power Dissipation Modeling, Active Power, Double Counting Clock Pin Power, Leakage Power, Other Attributes in Cell Library, Area Specification, Function Specification, SDF Condition, Characterization and Operating Conditions, What is the Process Variable, Derating using K-factors, Library Units.		
3	**Interconnect Parasitics**: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation of Extracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets. **Delay Calculation**: Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation.	11	L1,L2, L3, L4
4	**Configuring the STA Environment**: What is the STA Environment? Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge_shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example C, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Specifying Inactive Signals, Breaking Timing Arcs in Cells, Point-to-Point Specification, Path Segmentation.	11	L1,L2, L3, L4
5	**Timing Verification**: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flipflop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip-flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across	10	L1,L2, L3, L4

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
	Clock Domains, Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks, Integer Multiples, Non-Integer Multiples, Phase Shifted.		

Note: Each Unit will have internal choice.

COURSE OUTCOMES

CO1 Evaluate the delay of any given digital circuits.

CO2 Prepare the resources to perform the static timing analysis using EDA tool.

CO3 Prepare timing constraints for the design based on the specification.

CO4 Generate the timing analysis report using EDA tool for different checks.

CO5 Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO4,PO5
CO2	PO2,PO3,PO4
CO3	PO3,PO4
CO4	PO3,PO4,PO5,
CO5	PO2,PO3,PO4,PO7
CO6	PO1,PO2,PO4,PO5,PO8,PO12

TEXT BOOK:

1. J. Bhasker, R Chadha, “Static Timing Analysis for Nanometer Designs: A Practical Approach”, Springer, 2009.

REFERENCE BOOKS/WEBLINKS:

1. Sridhar Gangadharan, Sanjay Churiwala, “Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)”, Springer, 2013.
2. Naresh Maheshwari and Sachin Sapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999.

Subject Title: **SYSTEM VERILOG PROGRAMMING**		
Subject Code: **LVS151**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives.

This course will enable the students to:

1. Understand digital system verification using object oriented methods
2. Learn the System Verilog language for digital system verification.
3. Create/build test benches for the basic design/methodology.
4. Use constrained random tests for verification
5. Understand concepts of functional coverage

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Verification Guidelines**: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components. **Data Types**: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	12	L1,L2, L3,
2	**Procedural Statements and Routines**: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Converting the test bench and design**: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	10	L1,L2, L3
3	**Randomization**: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control. and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	10	L1,L2, L3, L4
4	**Threads and Interprocess Communication**: Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.	10	L1,L2, L3, L4
5	**Functional Coverage**: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	10	L1,L2, L3, L4

Note: Each Unit will have internal choice.

COURSE OUTCOMES: After studying this course, students will be able to:

CO1 Write test benches for moderately complex digital circuits

CO2 Use System Verilog language to implement digital systems

CO3 Appreciate functional coverage

CO4 Apply constrained random tests benches using System Verilog

CO5 Analyze a verification case and apply System Verilog to verify the design

CO6 VLSI Verification software's effectively to implement and verify digital systems

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7,PO8
CO5	PO3,PO4
CO6	PO3,PO4,PO5

TEXT BOOK

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.

REFERENCE BOOKS/WEBLINKS

1. Stuart Sutherland, Simon Davidmann, Peter Flake, ―System Verilog for Design A guide to using system verilog for Hardware design and modelling, Springer Publications, 2nd Edition, 2006.

Subject Title: **VLSI DESIGN VERIFICATION AND TESTING**		
Subject Code: **LVS22**	No. of Credits**:3=4:0:0(LTP)**	No. of lecture hours/week **: 04**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **40+10+50=100**	Total No. of Contact Hours **:52**

Course Learning Objectives

1 Model and simulate different types of faults in digital circuits at the gate level.

2 Establish equivalence and dominance relationships of faults in a circuit.

3 Critique and compare automatic test pattern generation algorithms with respect to search space, speed, fault coverage and other criteria.

4 Understand the meaning of physical design and static timing analysis.

5 Understand about BICMOS and other technologies.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Introduction to Testing:** Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults. **Test Generation for Combinational Logic Circuits:** Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits. **[TEXT1]**	10	L2,L3
2	**Design of Testable Sequential Circuits:** Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Cross Check, Boundary Scan. Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.**[TEXT1]**	12	L3, L4
3	**Importance of Design Verification:** What is verification? What is attest bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification. **Verification Tools:** Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and esource code, code reviews. Simulators: Stimulus and response, Event	09	L2,L3

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
	based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.**[TEXT2]**		
4	**The verification plan:** The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. **[TEXT2]**	12	L1,L2
5	**Static Timing Verification**: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, false paths, Timing models.**[TEXT2]**	09	L2,L3

Note: Each Unit will have internal choice.

COURSE OUTCOMES:

CO1 Illustrate the fundamentals principles of VLSI testing

CO2 Identify the testing code for the digital circuits

CO3 Compare the difference between testing and verification

CO4 Analyse the various VLSI testing and verification concepts.

CO5 Construct the Levels of verification and Plan

Course outcome and program outcome mapping

CO1 PO1,PO2

CO2 PO2,PO3,PO4

CO3 PO2,PO3,PO4,PO5

CO4 PO7,PO8

CO5 PO3,PO4

TEXT BOOK

1. P K Lala, “Digital Circuit Testing and Testability” , First Edition, Academic Press, 1997
2. M L Bushnell and V D Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits” , First Edition, Kluwar Academic Publishers, New York, 2002

REFERENCE BOOKS/WEBLINKS

1. Janick Bergeron, “Writing Test Benches: Functional Verification of HDL Models” , Second Edition, Kluwar Academic Publishers, 2003
2. Bhasker J, Chadha and Rakesh, “Static Timing Analysis for Nanometer Designs-A Practical Approach” , First Edition, Springer Publications, 2009